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| 10/781,692 | 02/20/2004 | Alex A. Lopez-Estrada | 42339-193224 | 3689 |

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VENABLE LLP
P.O. BOX 34385
WASHINGTON, DC 20043-9998

| EXAMINER | |
|---|---|
| MCFADDEN, MICHAEL B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/781,692 | LOPEZ-ESTRADA, ALEX A. | |
| | Examiner | Art Unit | |
| | Michael B. McFadden | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,8-17,20-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-17,20-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

1. Claims 7, 18, 19, 23, and 25-27 are cancelled.

2. Claims 1-6, 8-17, 20-22, and 24 are pending in the Application.

### *Response to Amendment*

3. Applicant's arguments filed on 08 September 2006 have been fully considered but they are not persuasive.

### *Objections to the Abstract*

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. Abstract fails to sufficiently describe disclosed invention. Proper correction is required.

## ***Objections to the Claims***

6. Claim 20 is objected to because of the following informalities: Claim 20 depends on cancelled claim 19. For the purposes of further examination the Office will assume that claim 20 should be dependant upon claim 17. Appropriate correction is required.

## ***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 9-12, 21, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kohn et al. (US Patent No. 6,006,312(herein after Kohn)).

9. **Regarding Claims 9, 10, 21, and 24,** Kohn discloses determining possible aliased locations in a memory comprising of a number of buffers; increasing a count when a buffer that is a possible aliased location is found; and storing data in the buffers at a location that is offset based on the count and a number of bytes selected for offset, wherein the offset is a product of the count and the number of bytes. **(Kohn: Figure 4 and 5, Column 6, Line 50 – Column 7, Line 11) Having a table of like the look aside buffer in the figures is how the system keeps track of possible locations. There are a limited number of spaces in the buffer therefore limiting the possible aliased locations. In Column 6, Lines 63-66 Kohn teaches offsetting the address by a**

**multiple of the virtual cache size. The virtual cache size is the count because that is the possible number of alias locations.**

10. **Regarding Claim 11,** Kohn discloses repeating steps a)-c). **(Kohn: Figures 7 and 8) The flow chart shows that the process is repeated.**

11. **Regarding Claim 12** Koch discloses determining a uniform size for the memory blocks, the size being large enough to accommodate the data and the offset and dividing the memory blocks into equal size. **(Kohn: Figure 2) The cache includes a memory block with enough space to accommodate the data and offset therefore determination step is inherent in that decision. The figure shows that the memory blocks are of equal size.**

12. **Regarding Claim 22,** Kohn discloses further comprising adding the offset to a pointer for respective memory blocks. **(Kohn: Column 6, Line 63 – Column 7, Line 4) The address is a pointer therefore when an offset is added it is added to a pointer for the memory blocks.**

## ***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-6, 8, 13-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohn et al. (US Patent No. 6,006,312(herein after Kohn)) as applied to claim 1 above, and further in view of Gibson et al. (US Patent No. 6,507,898(herein after Gibson))

15. **Regarding Claims 1, 13, and 15-17,** Kohn discloses computing a number of aliased address locations in a memory including a number of memory blocks; wherein computing the number of aliased address location based on at least one of a number of memory blocks, an intended size for the memory blocks, and an aliasing range.

**Having a table of like the look aside buffer in the figures is how the system keeps track of possible locations. There are a limited number of spaces in the buffer therefore limiting the possible aliased locations. In Column 6, Lines 63-66 Kohn teaches offsetting the address by a multiple of the virtual cache size. The virtual cache size is the count because that is the possible number of alias locations.**

Kohn fails to disclose allocating extra memory to the memory blocks based on the number of aliased address locations to obtain a new size for the memory blocks, computing a second number of aliased address locations based on the new size for the memory blocks, and computing an offset for data within the memory blocks based on the second number of aliased address locations. Wherein allocating extra memory to the memory blocks is based on at least one of the number of aliased address locations, a line size, and a line offset.

Gibson discloses allocating extra memory to the memory blocks based on the number of aliased address locations to obtain a new size for the memory blocks **(Gibson: Column 13, Line 55 – Column 14, Line 6)**, computing a second number of aliased address locations based on the new size for the memory blocks, and computing an offset for data within the memory blocks based on the second number of aliased address locations. **(Gibson: Column 85, Lines 56-62)** Wherein allocating extra memory to the memory blocks is based on at least one of the number of aliased address locations, a line size, and a line offset. **(Gibson: Column 13, Line 55 – Column 14, Line 6)**

**The second number of blocks would be calculated in the way that the first were.**

Kohn and Gibson are analogous art because they are from the same field of endeavor, cache memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to take the reconfigurable offset and dynamic memory of Gibson and use them in the memory system of Kohn.

The motivation for doing so would have been to create a versatile memory that can be used in many situations and for multiple applications.

Therefore it would have been obvious to combine the reconfigurable offset and dynamic memory of Gibson with the memory system of Kohn for the benefit of a versatile memory system to obtain the invention specified in claim 9.

16. **Regarding Claims 2 and 6** Koch discloses determining a uniform size for the memory blocks, the size being large enough to accommodate the data and the offset and dividing the memory blocks into equal size. **(Kohn: Figure 2) The cache includes a memory block with enough space to accommodate the data and offset therefore determination step is inherent in that decision. The figure shows that the memory blocks are of equal size.**

17. **Regarding Claim 3,** Kohn discloses wherein the memory blocks are buffers. **(Kohn: Figure 1) A cache is a buffer.**

18. **Regarding Claim 4,** Kohn fails to disclose wherein the buffer is a ring buffer.

Gibson discloses wherein the buffer is a ring buffer.

**(Gibson: Column 13, Lines 51-54)**

Kohn and Gibson are analogous art because they are from the same field of endeavor, cache memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the ring buffer of Gibson in Kohn.

The motivation for doing so would have been that a ring buffer is an efficient way to make use of a predefined memory hierarchy during the data reuse step. Also a ring buffer is an effective way to provide useful information after a failure.

Therefore it would have been obvious to a person of ordinary skill in the art to include the ring buffer of Gibson in the memory system of Kohn for the benefit of efficiently making use of a predefined memory hierarchy during the data reuse step and

effectively providing useful information after a failure to obtain the invention as specified in claim 4.

19. **Regarding Claim 5,** Kohn discloses wherein the buffer is a linear buffer. **(Kohn: Column 6, Lines 39-42 and Column 8, Lines 16-17)**

20. **Regarding Claims 8, 14, and 20,** Kohn discloses further comprising adding the offset to a pointer for respective memory blocks. **(Kohn: Column 6, Line 63 – Column 7, Line 4) The address is a pointer therefore when an offset is added it is added to a pointer for the memory blocks.**

## ***Response to Arguments***

21. Applicant's arguments with respect to claims 1, 17, and 21 have been considered but are moot in view of the new ground(s) of rejection.

22. Applicant's arguments filed 08 September 2006 have been fully considered but they are not persuasive.

23. **Regarding Claims 9 and 21,** Applicant contends that Kohn fails to disclose storing data in buffers at a location that is offset based on count and a number of bits selected for the offset. **However, as previously stated in the rejection, (Kohn: Figure 4 and 5, Column 6, Line 50 – Column 7, Line 11) having a table of like the look aside buffer in the figures is how the system keeps track of possible locations. There are a limited number of spaces in the buffer therefore limiting the possible aliased locations. In Column 6, Lines 63-66 Kohn teaches offsetting the address**

**by a multiple of the virtual cache size. The virtual cache size is the count because that is the possible number of alias locations. The data is inherently stored buffers. Also, with the data being offset there is inherently a number of bits selected for the offset.**

24. **Regarding Claims 1, 7, and 13,** Applicant contends that Gibson fails to disclose allocating extra memory blocks within a queue based on at least one of the number of memory blocks, an intended size for the memory blocks, and an aliasing range address. **However, as previously stated in the rejection, (Gibson: Column 13, Line 55 – Column 14, Line 6) Gibson teaches allocating memory and allowing the system to adapt automatically to the amount of memory available, the number of memory blocks.**

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

## ***Conclusion***

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sam Sough can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBM
11/13/2006

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
11/22/06